





Model Name: 7VM400M-RZ

Revision 1.0

SHEET	TITLE
1	BOM & PCB MODIFY HISTORY
2	COVER SHEET
3	BLOCK DIAGRAM
4,5	AMD CPU SOCKET A
6,7,8	KM400 HOST; DDR; AGP,VLINK,POWER/GOUND
9	CLOCK GENERATOR (ICS950913CF)
10,11,12	VT8235 (SOUTH BIRDGE)
13,14	DDR SDRAM DIMMS 1,2 DDR TERMINATION
15	AGP SLOT
16	PCI SLOT 1,2,3
17	IDE,USB
18	LPCIO_IT8705
19	BIOS
20	COM,PRT,FDD,KB/MS,IR
21	AC 97 VT1617 CODEC
22	AUDIO JACK,GAME PORT
23	VT6103 & USB CONNECTOR
24	PANEL,STR LED,FANS
25	DDR POWER
26	ATX CONN,3VDUAL,VDDQ DC POWER
27	VCORE PHASE PWM FAIRCHILD FAN5091M
28	VID,FID CONTROL

		COMPONENT SIDE (1 oz. Copper)
		GND SIDE (1 oz. Copper)
		VCC SIDE (1 oz. Copper)
		SOLDER SIDE (1 oz. Copper)
GIGABYTE		
Title COVER SHEET		
Size Custom	Document Number 7VM400M-RZ	Rev 1.0
Date: 星期 二 四月 27, 2004	Sheet 1 of 28	

Version:1.0

Component value change history

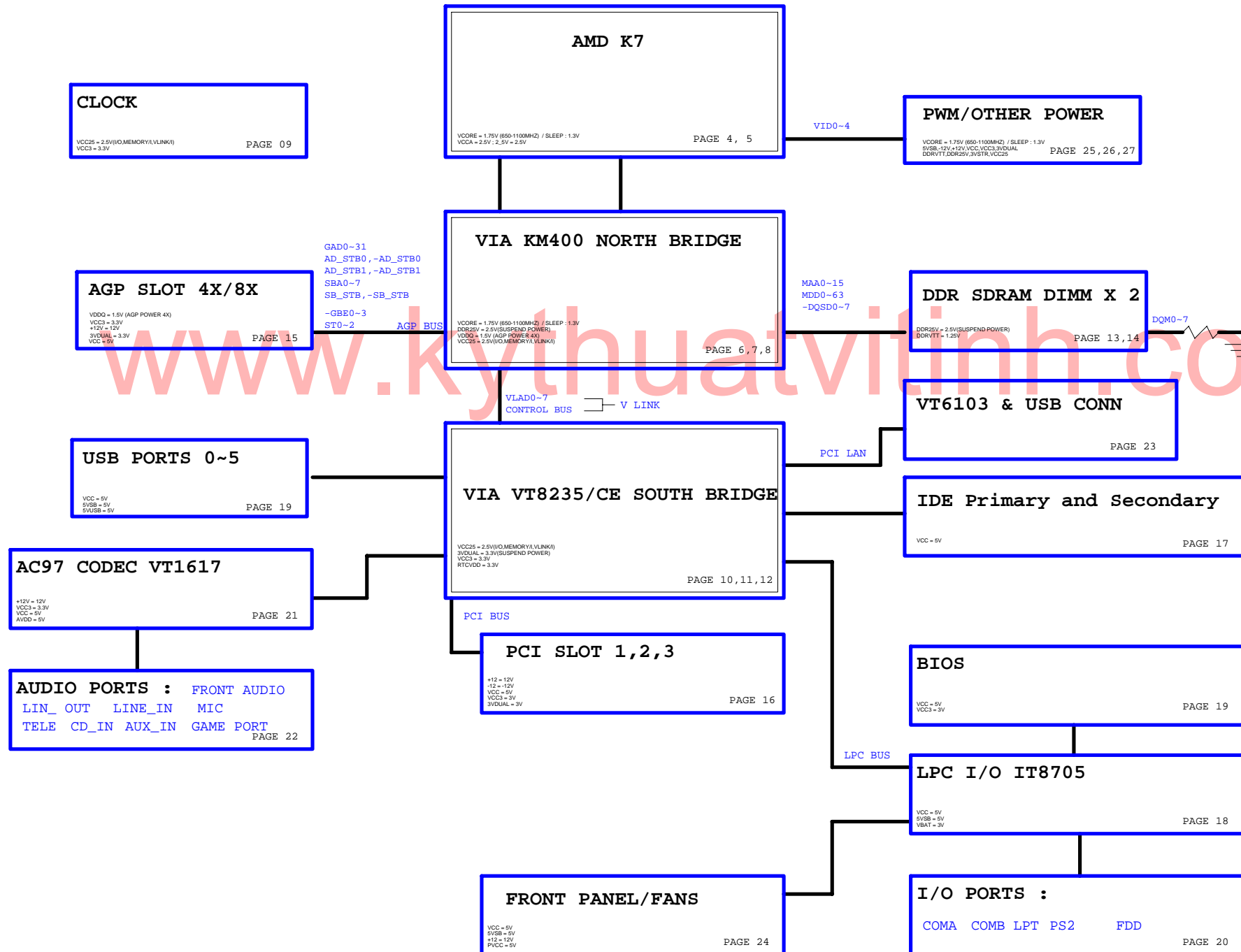
2004.01.13

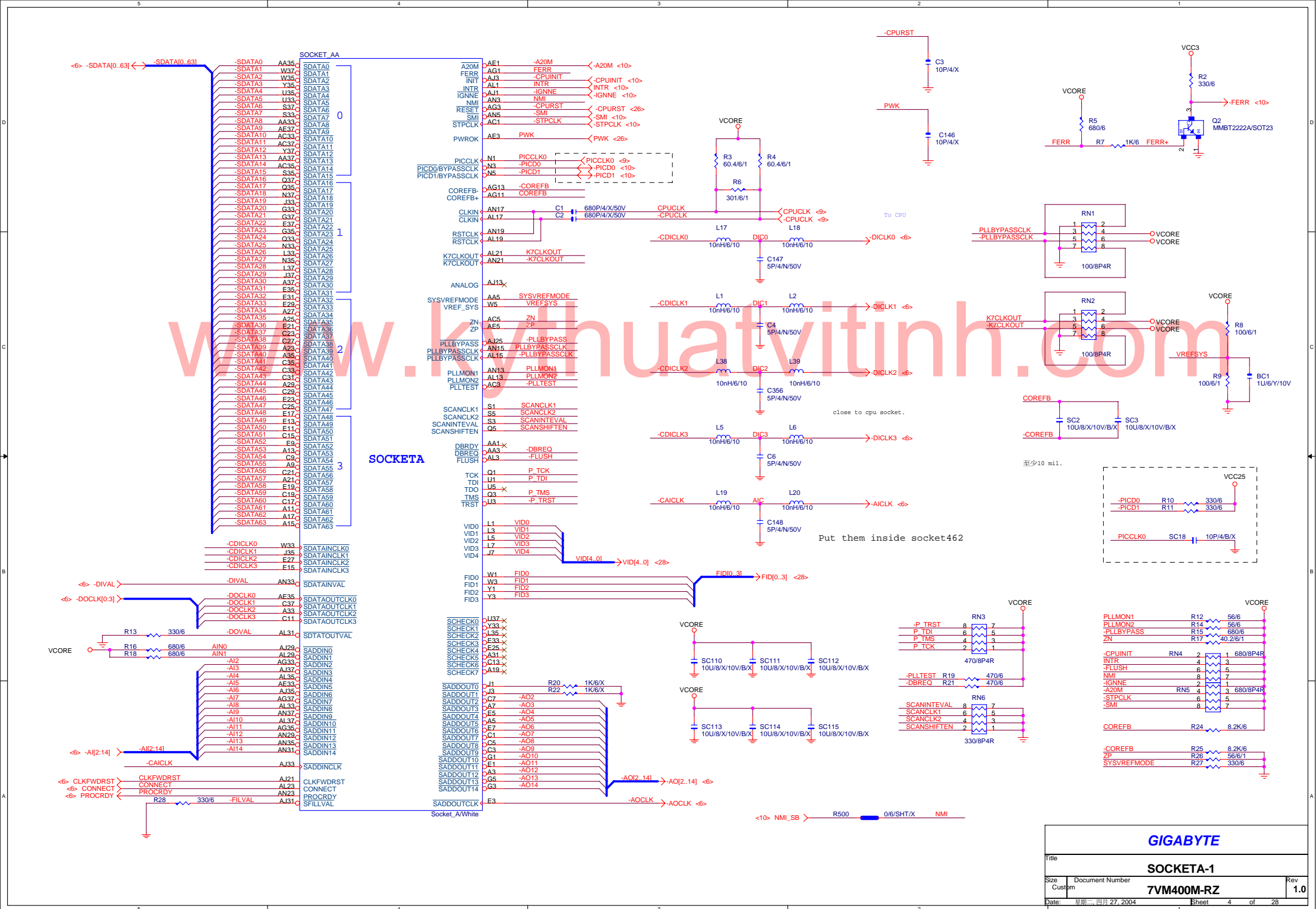
[illegible]

Circuit or PCB layout change for next version

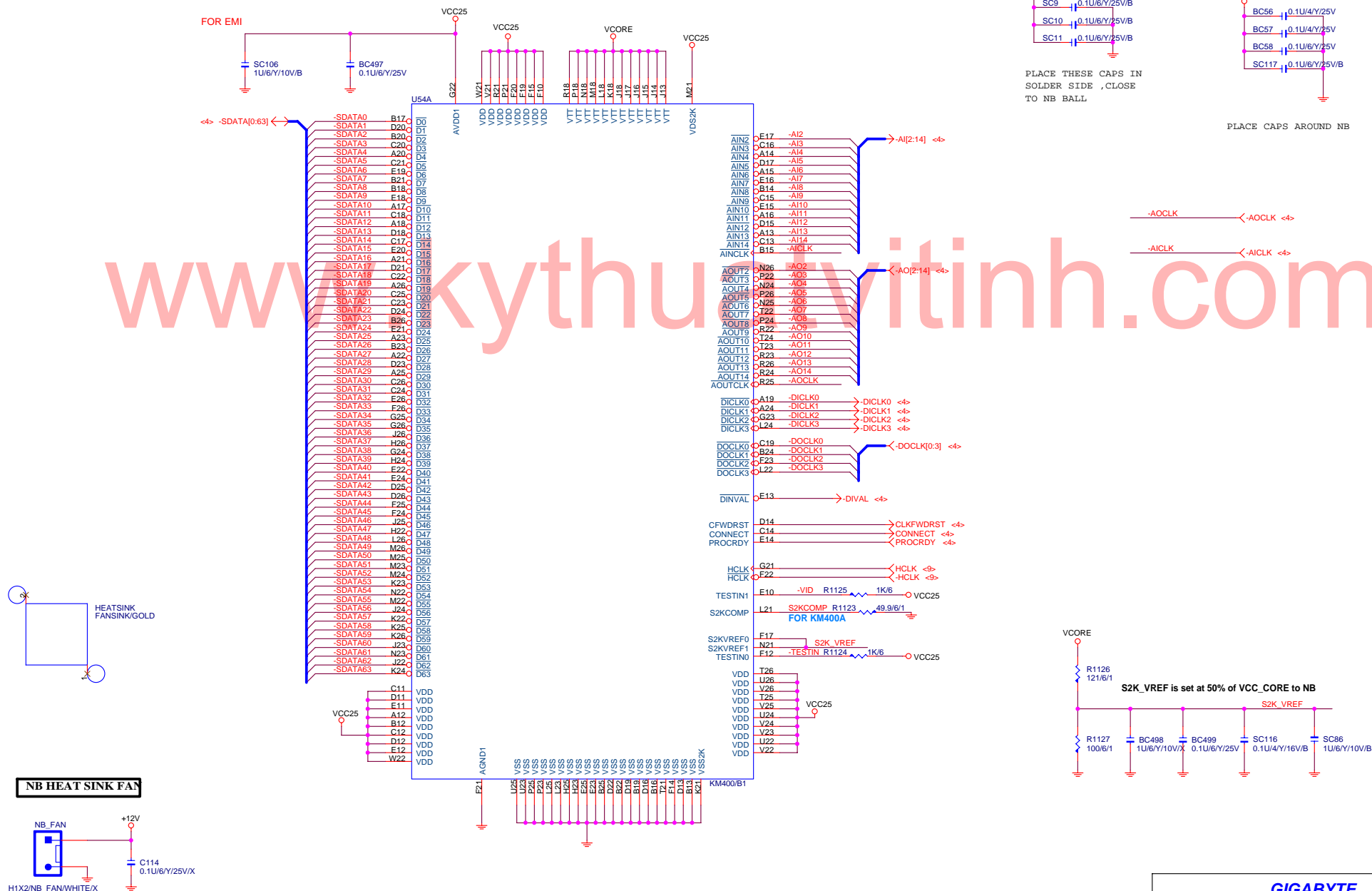
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7VM400M-RZ BLOCK DIAGRAM



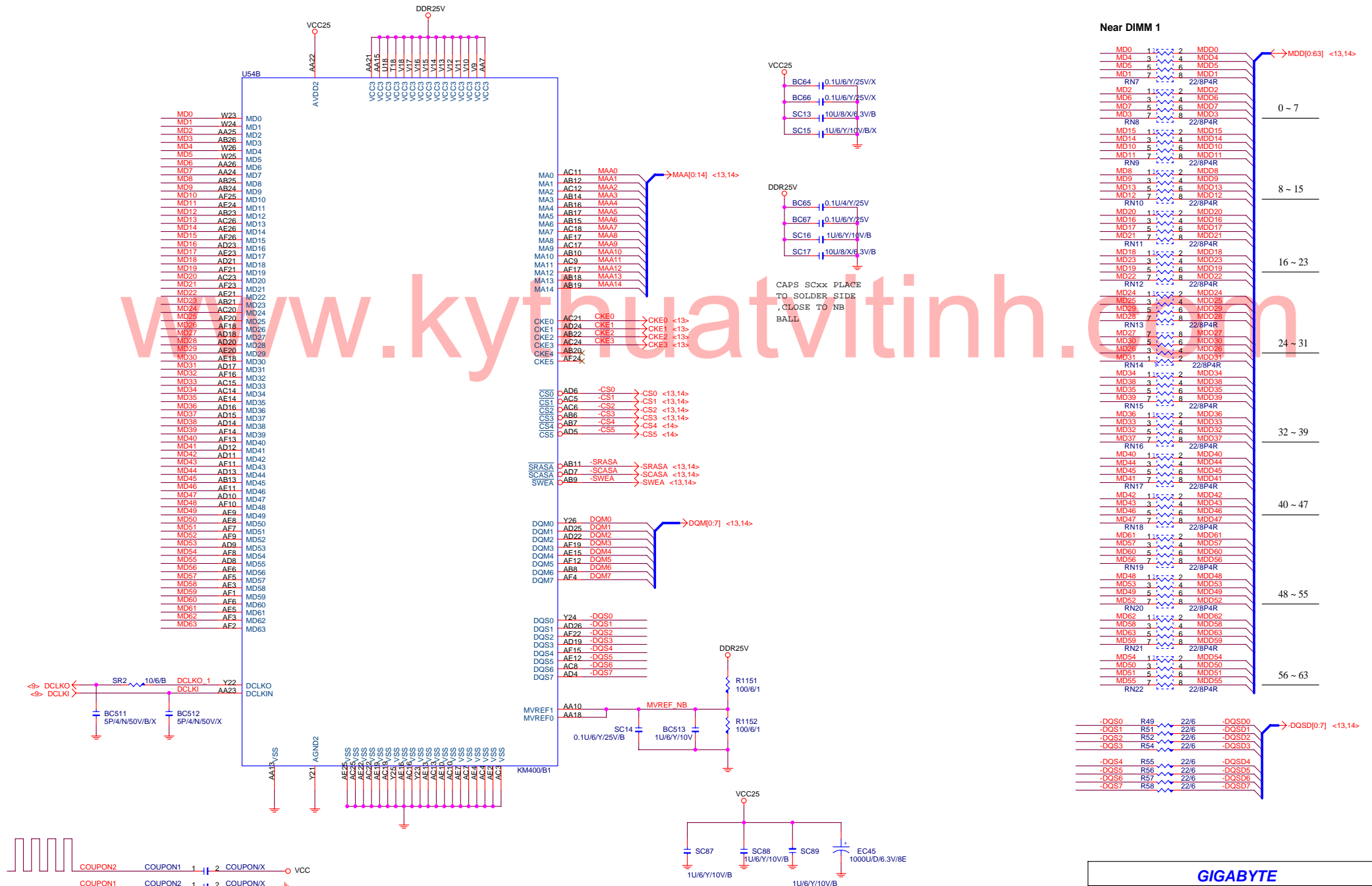


VT-KM400A (S2K BUS)

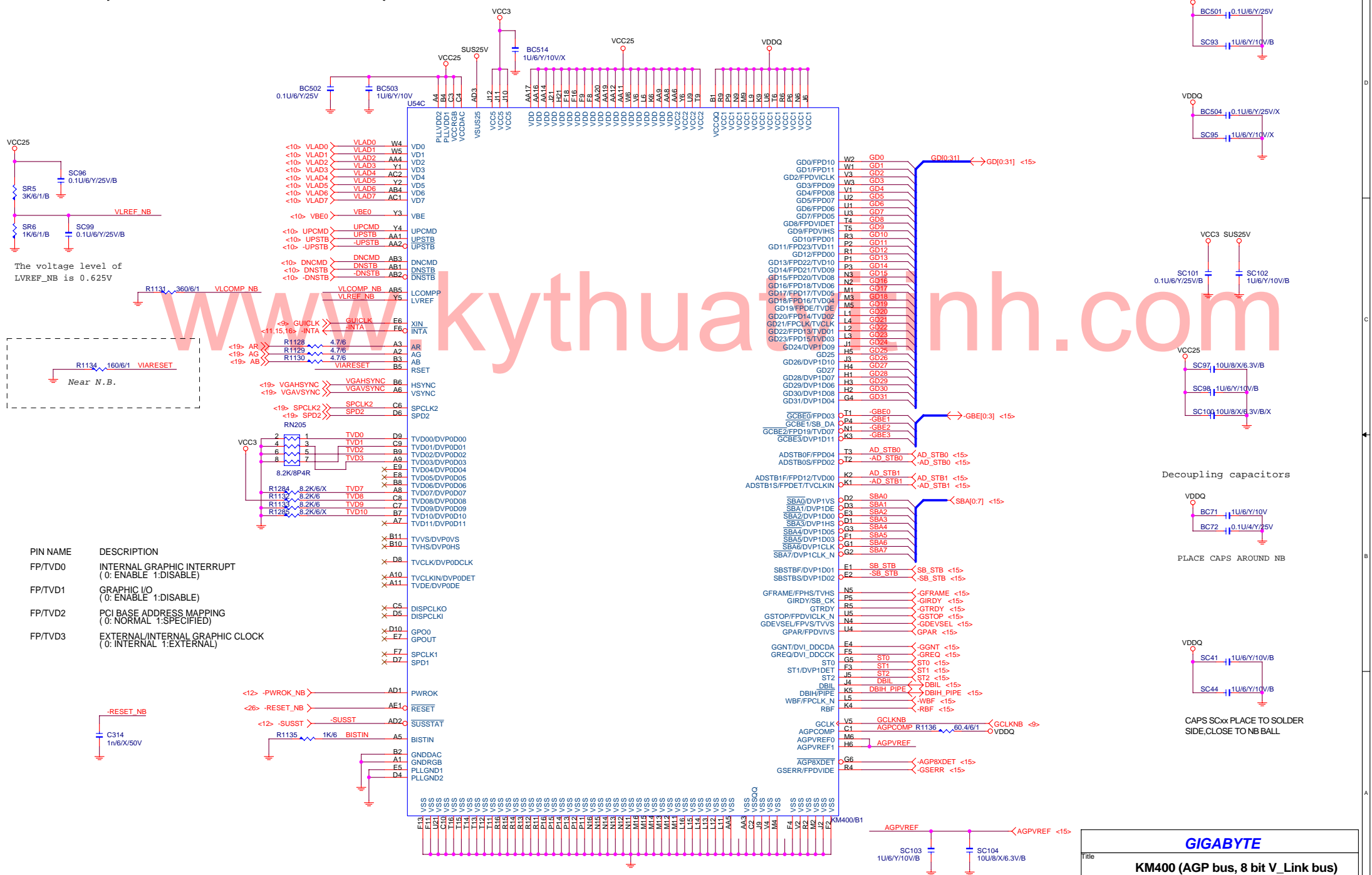


VT-KM400 (DDR BUS)

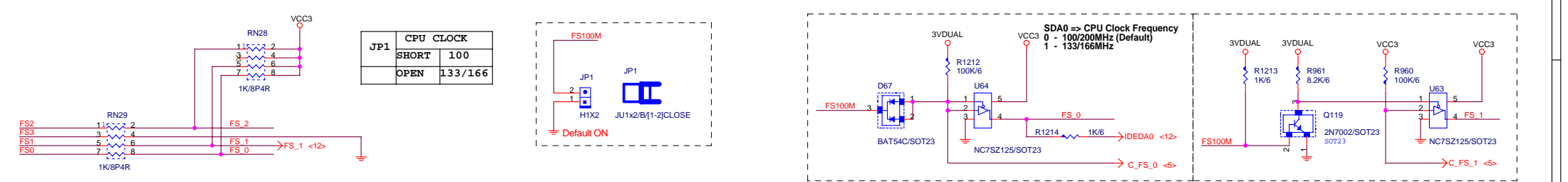
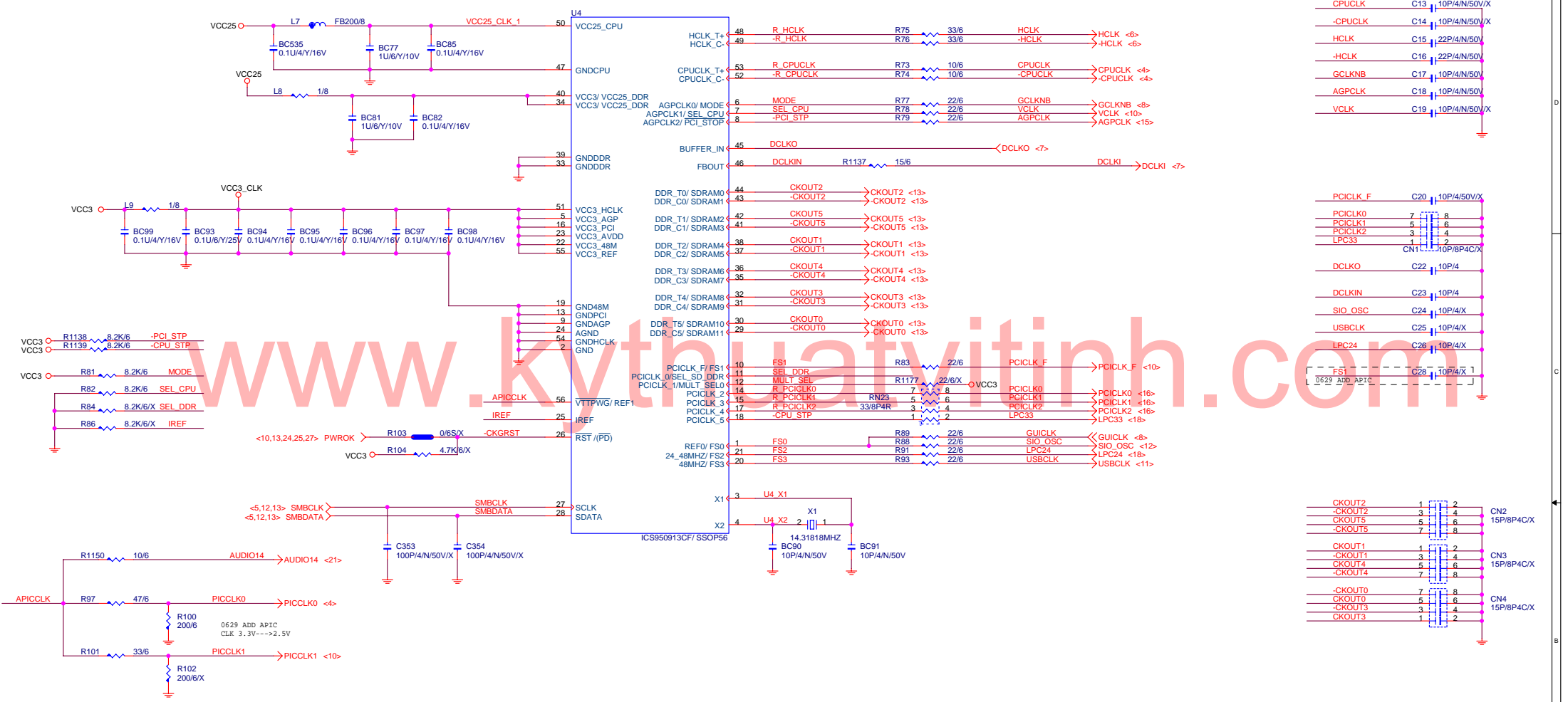
DDR MD DAMPPING



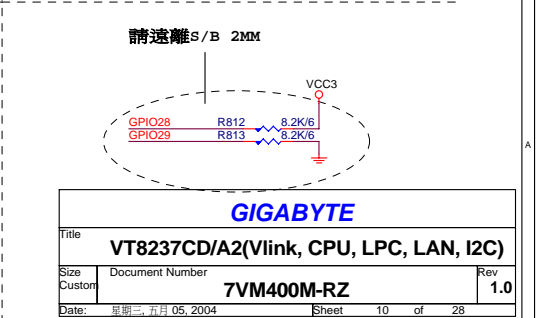
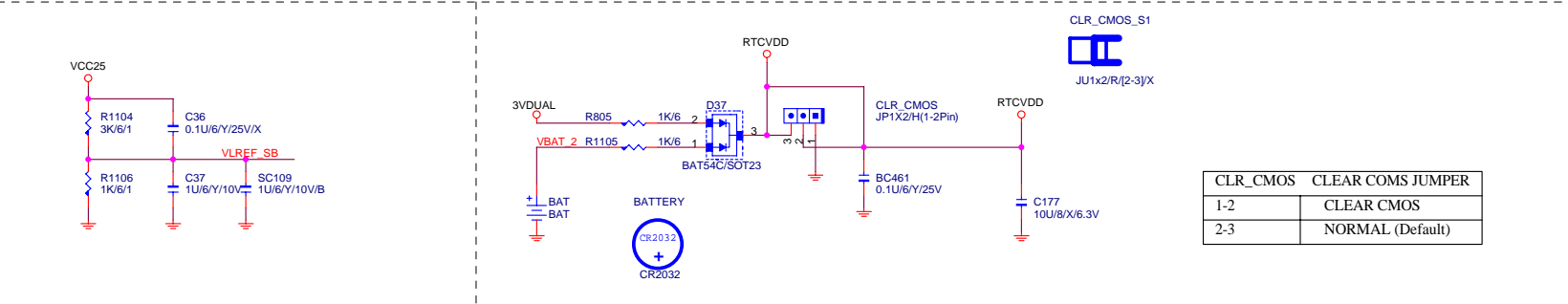
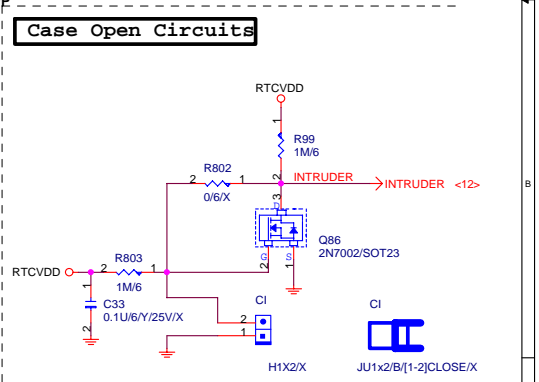
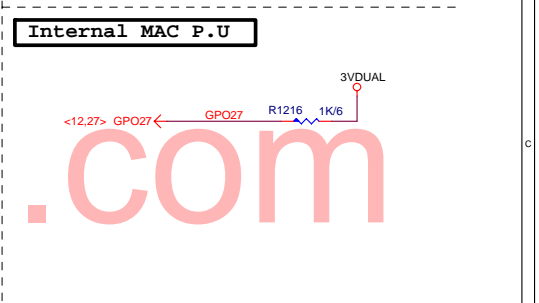
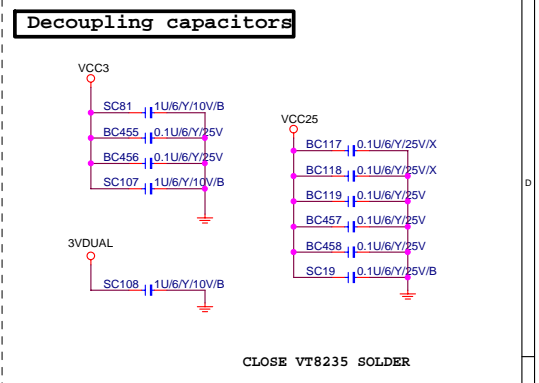
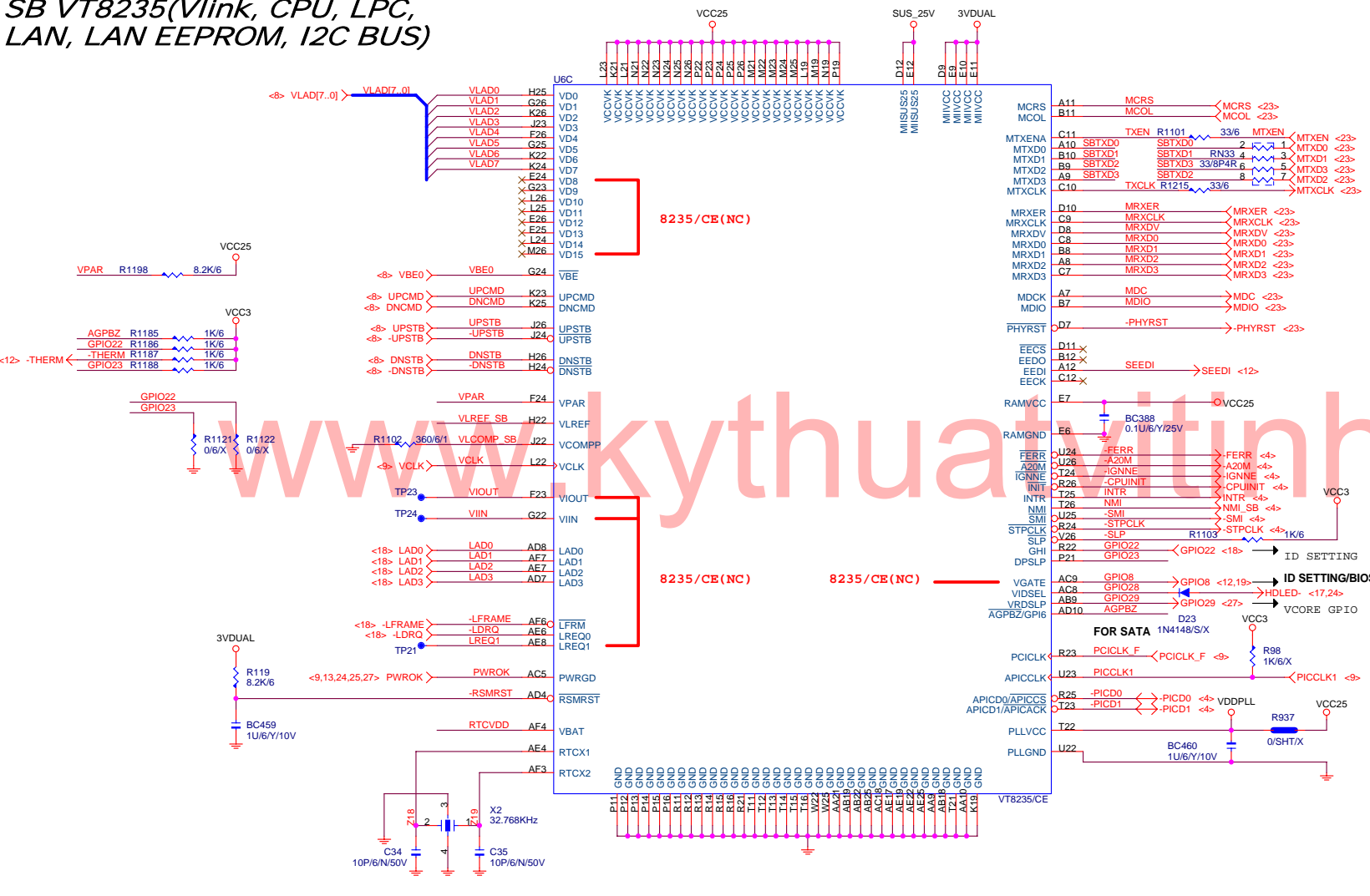
KM400A (AGP bus, 8 bit V_Link bus)



CLOCK GENERATOR



SB VT8235(Vlink, CPU, LPC, LAN, LAN EEPROM, I2C BUS)



CLR_CMOS CLEAR COMS JUMPER	
1-2	CLEAR CMOS
2-3	NORMAL (Default)

GIGABYTE

VT8237CD/A2(Vlink, CPU, LPC, LAN, I2C)

7VM400M-RZ

Rev 1.0

Document Number

Size Custom

Date: 五月 05, 2004

Sheet 10 of 28

AD23 L4
AD24 L1
AD25 M2
AD26 M1
AD27 P4
AD28 N2
AD29 N1
AD30 P1
AD31 P2

AD22 L4
AD23 L1
AD24 M2
AD25 M1
AD26 P4
AD27 N2
AD28 N1
AD29 P1
AD30 P2
AD31

USBP0+ D20
USBP1+ A20
USBP1- B20
USBP2+ E18
USBP2- D18
USBP3+ A18
USBP3- B18

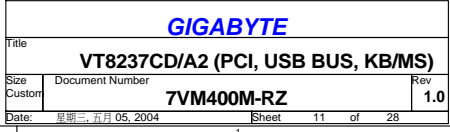
D23
C22
1U/6V/10V
1U/6V/10VX

USBDT0+
USBDT0-
USBDT1+
USBDT1-
USBDT2+
USBDT2-
USBDT3+
USBDT3-

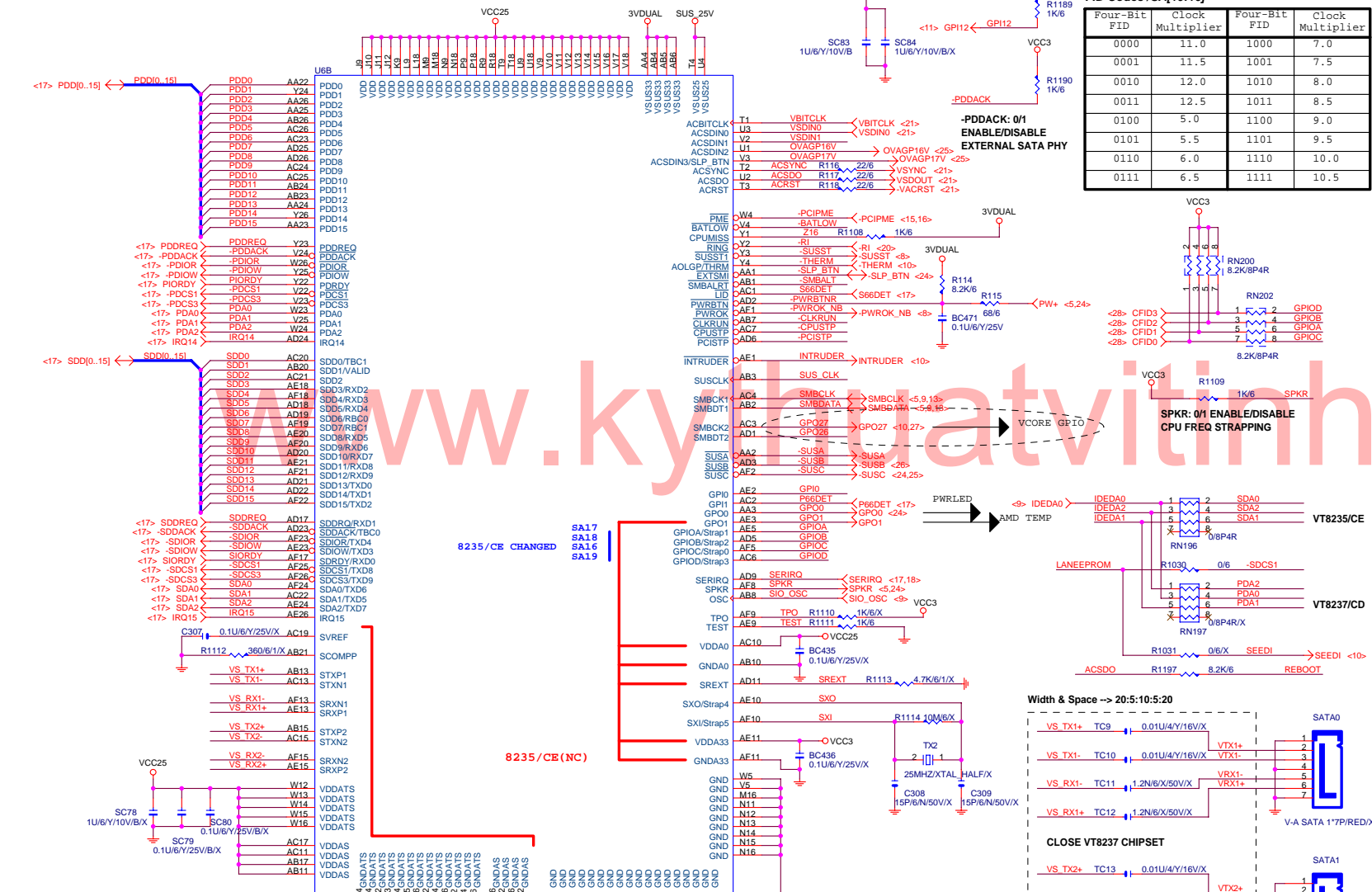
USBDT4+ <17>
USBDT5+ <17>
USBDT5+ <17>

RN173
15K/8P4R

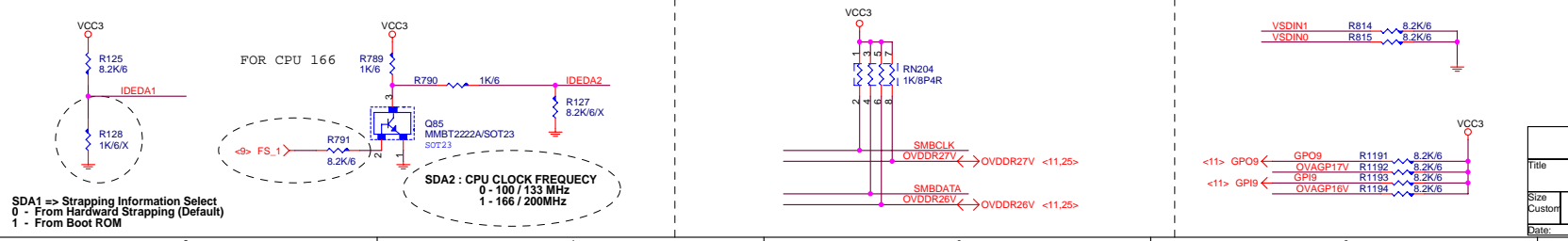
<10>-C-BE0
-C-BE0
E2
C-BE0



SB VT8235 (SATA,IDE, AC97, POWER MANAGEMENT, PGIO)



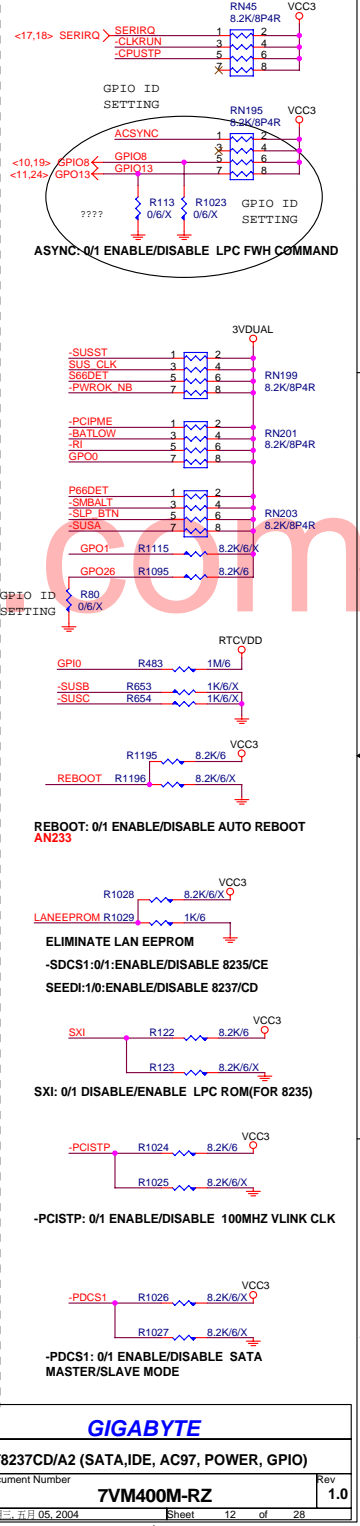
- VT8237 INTERNAL IDSEL LIST:**
- 1.AD26:SATA
 - 2.AD27:USB2.0
 - 3.AD28:S.B(USB1.1)
 - 4.AD29:LAN



Power Up Strappings :

FID Codes /SA[19:16]

Four-Bit FID	Clock Multiplier	Four-Bit FID	Clock Multiplier
0000	11.0	1000	7.0
0001	11.5	1001	7.5
0010	12.0	1010	8.0
0011	12.5	1011	8.5
0100	5.0	1100	9.0
0101	5.5	1101	9.5
0110	6.0	1110	10.0
0111	6.5	1111	10.5



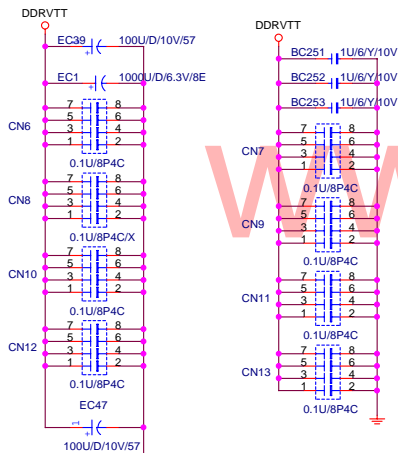
GIGABYTE

Title: VT8237CD/A2 (SATA,IDE, AC97, POWER, GPIO)

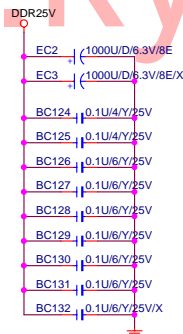
Size: Custom Document Number: 7VM400M-RZ Rev: 1.0

Date: 2004.05.05 Sheet: 12 of 28

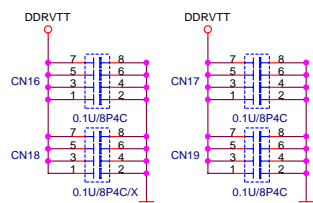
DDRVTT Decouple



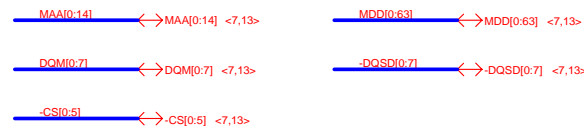
DDR25V Decouple



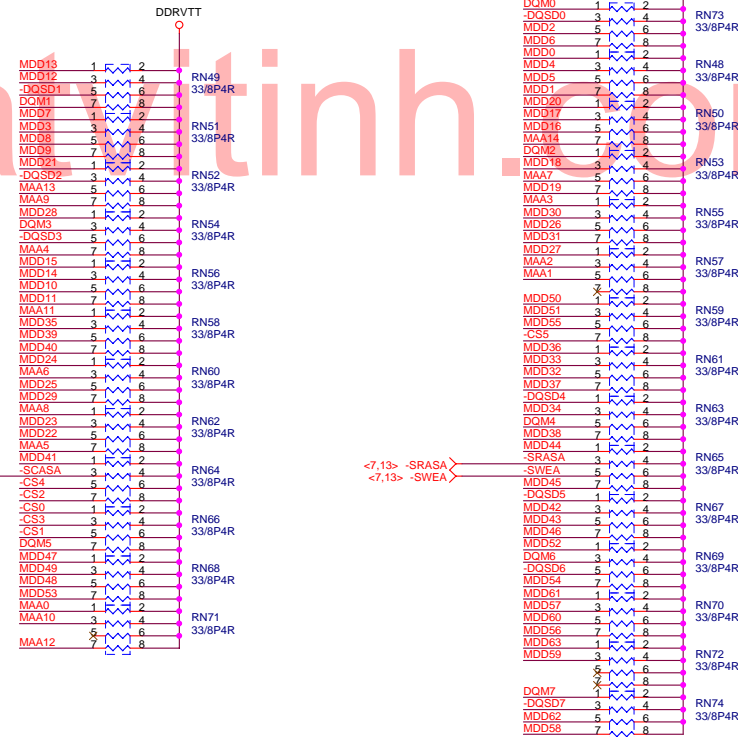
NOTE: Place Detribute 4 pcs
per DDR module.



NOTE: Place these decoupling
capacitors close to VTT_MEM
termination resistors. (one
decoupling coapcitor for each
two R-packs)



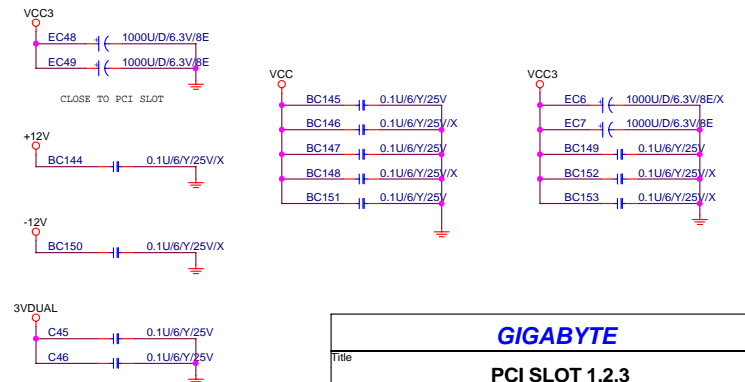
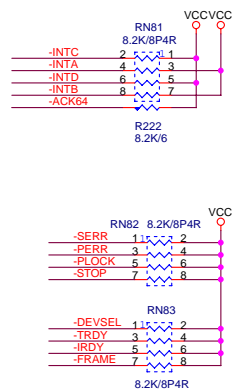
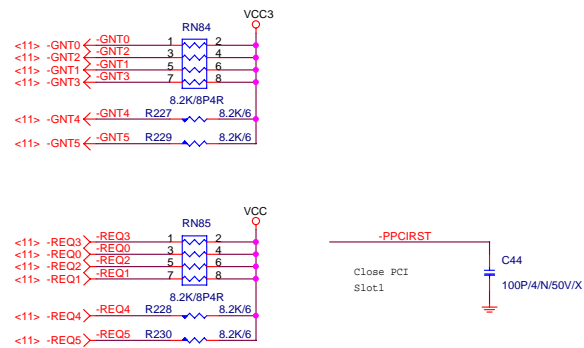
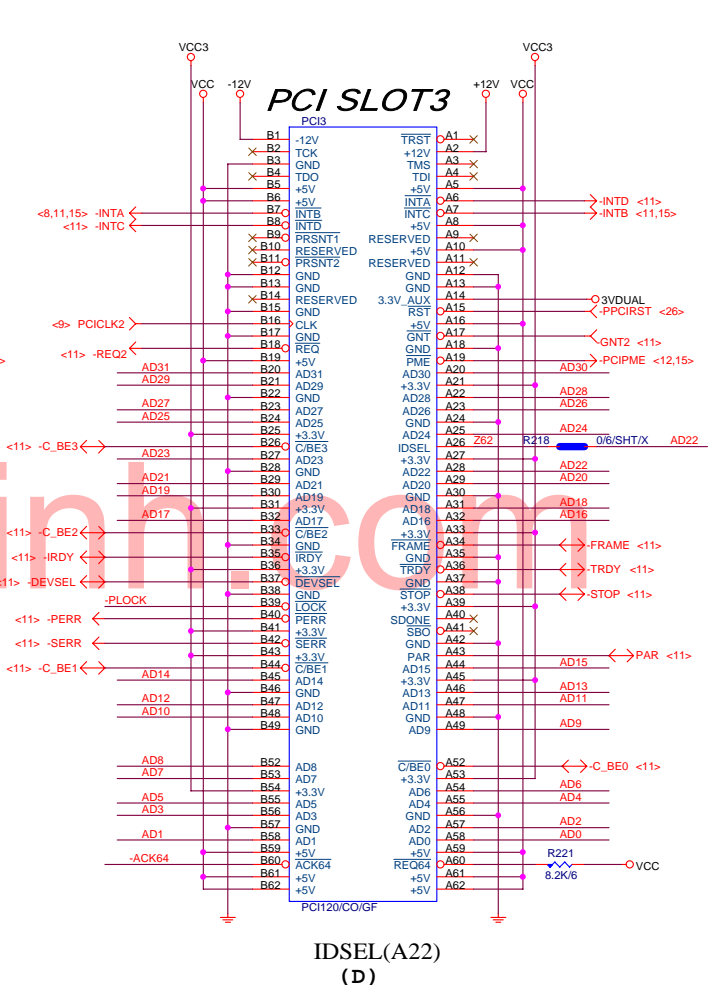
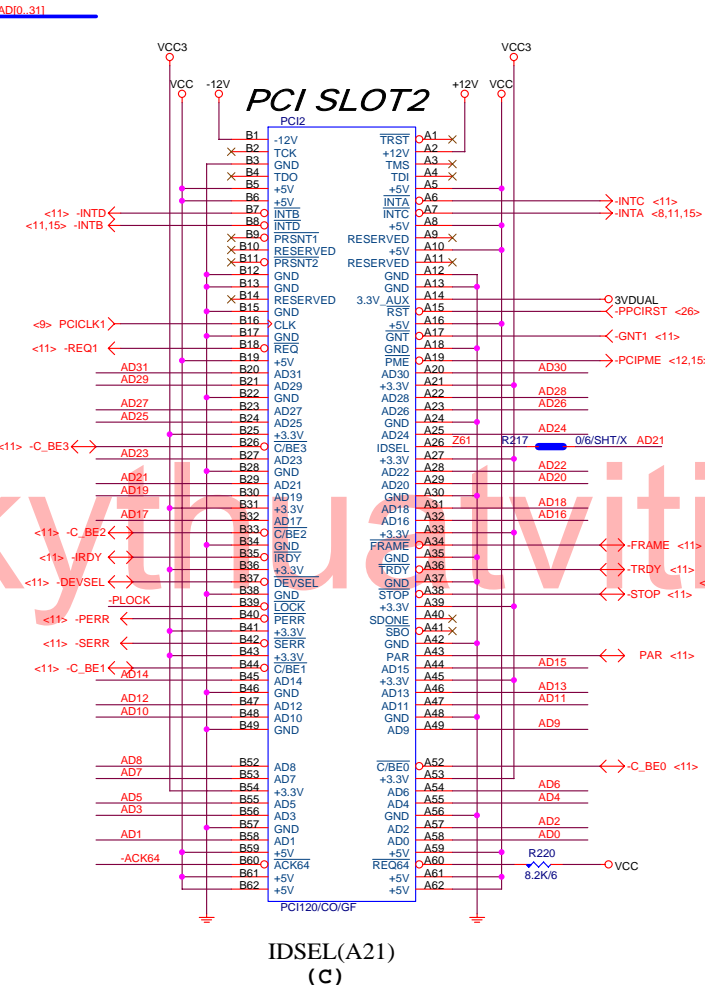
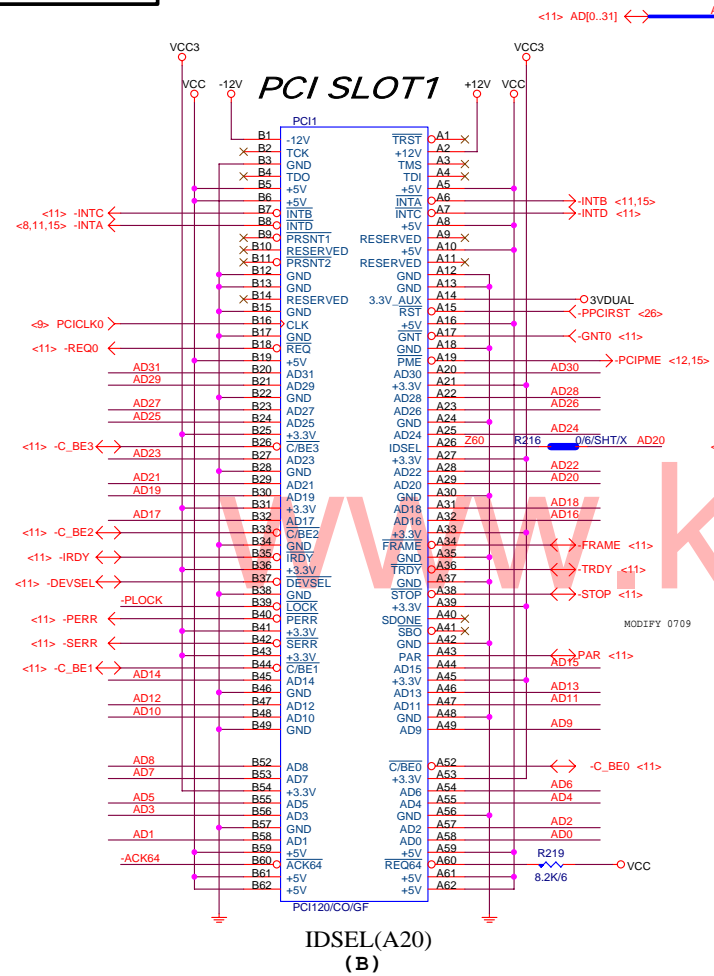
DDR TERMINATION



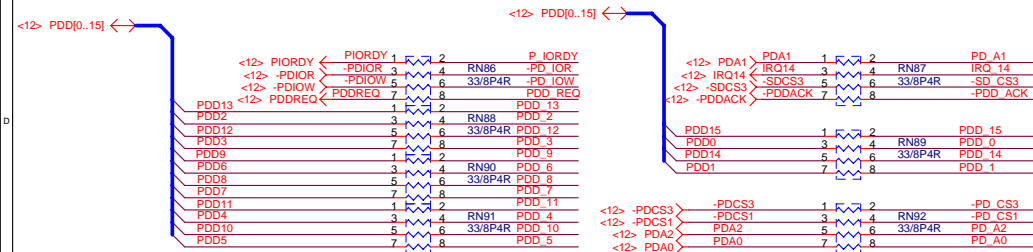
GIGABYTE

Title			
DDR TERMINATION			
Size	Document Number	Rev	
Custom	7VM400M-RZ	1.0	
Date:	星期三, 五月 05, 2004	Sheet	14 of 28

PCI SLOT 1,2,3

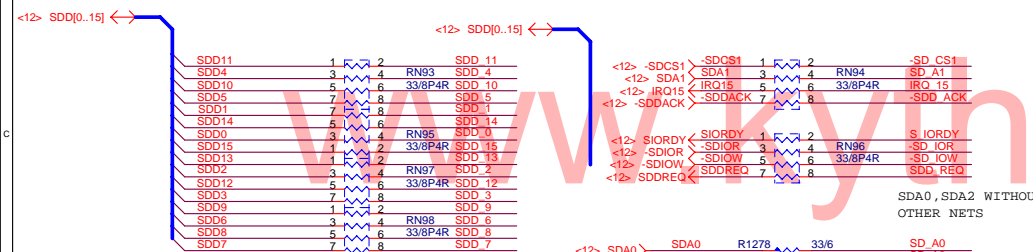


PRIMARY IDE

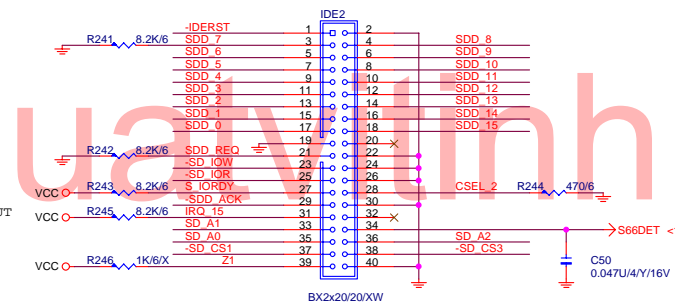
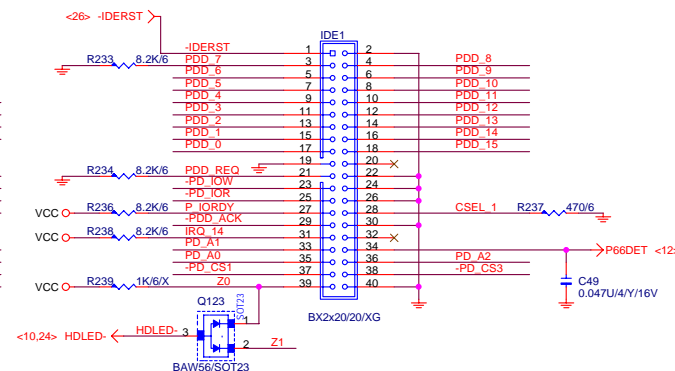


These resistor should placed near South Bridge

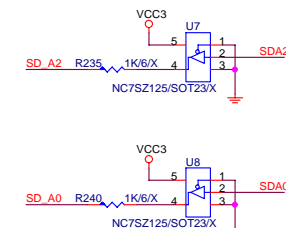
SECONDARY IDE



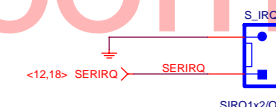
These resistor should placed near South Bridge



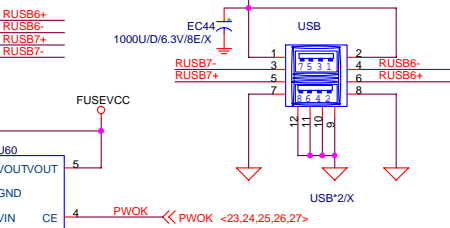
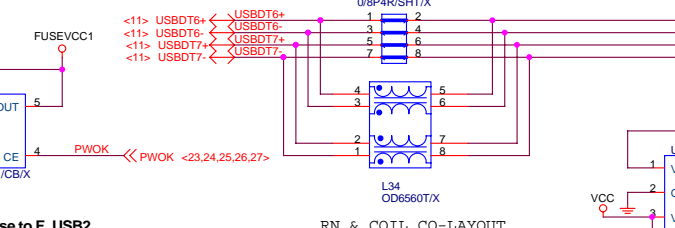
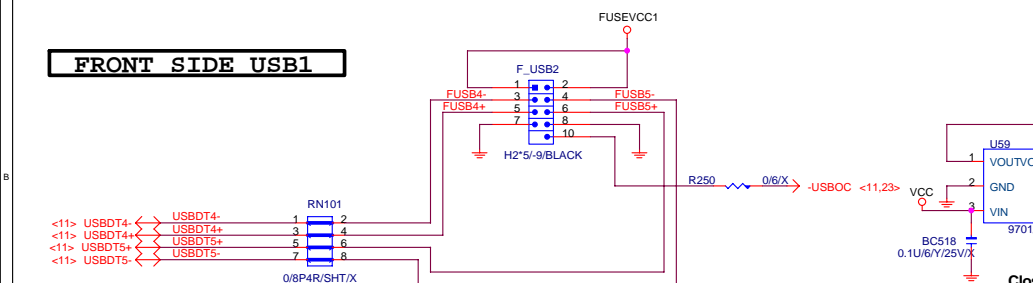
CD,DVD ROM STRAPPING ISSUE



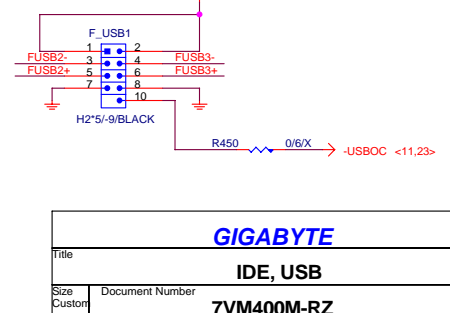
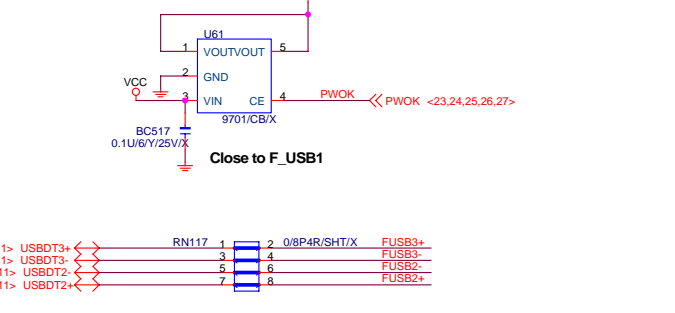
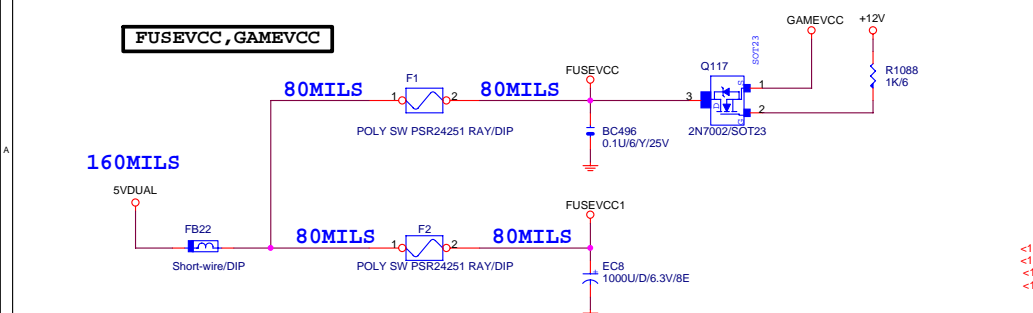
SIRQ



FRONT SIDE USB1



FUSEVCC, GAMEVCC

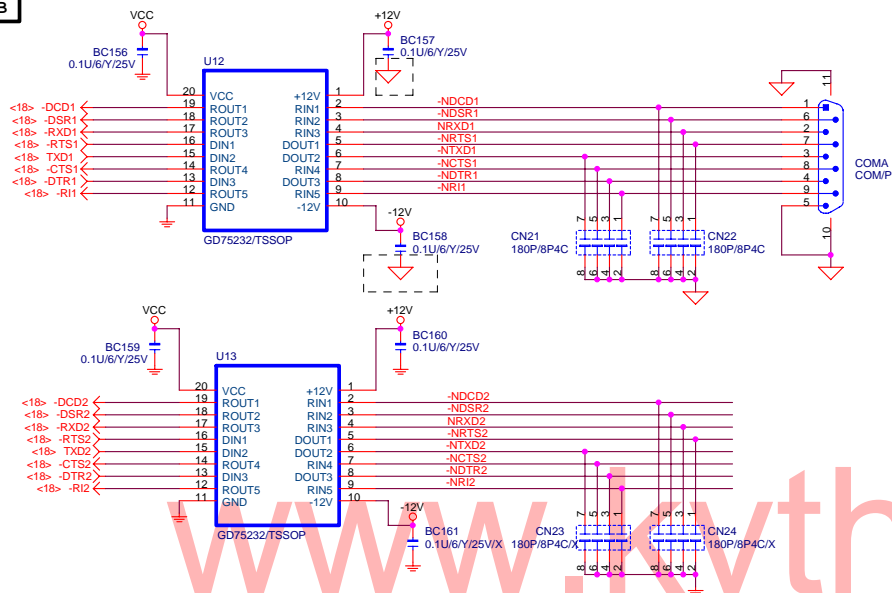


GIGABYTE

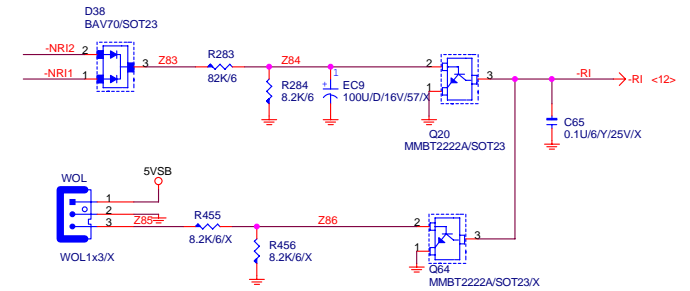
IDE, USB

Title	Document Number	Rev
Size	7VM400M-RZ	1.0
Custom		
Date:	星期二, 四月 27, 2004	Sheet 17 of 28

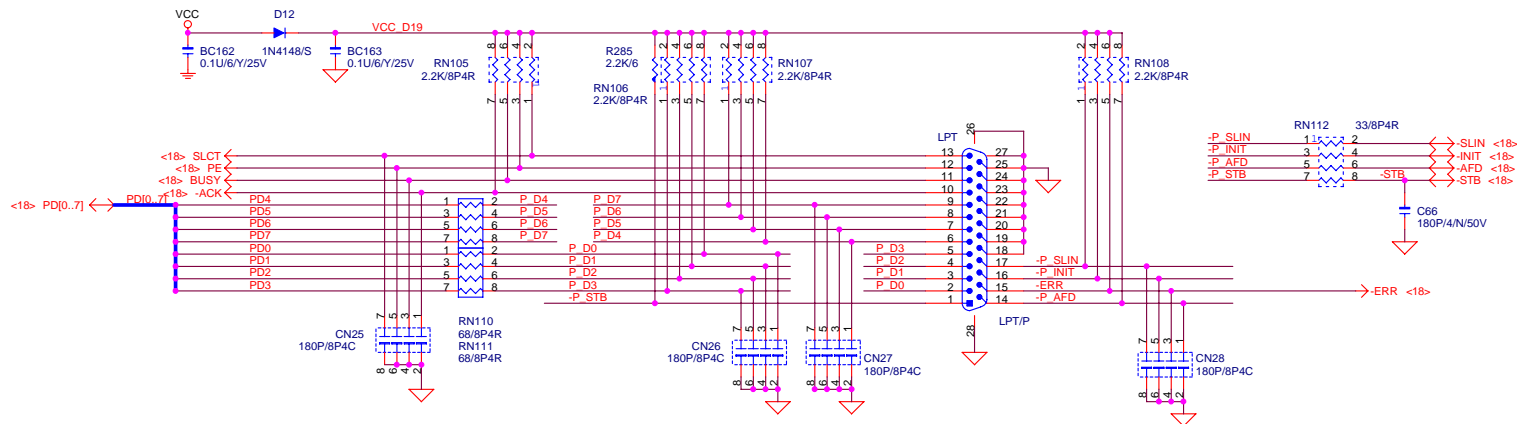
COM A,B



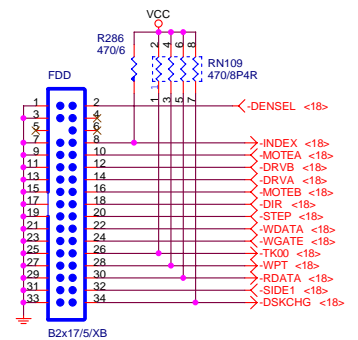
WAKE UP



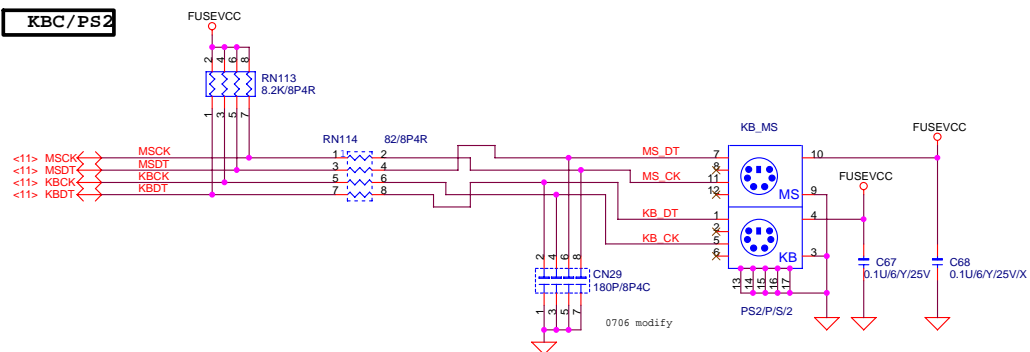
LPT

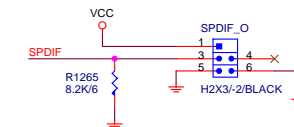
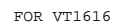
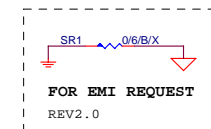


FDD

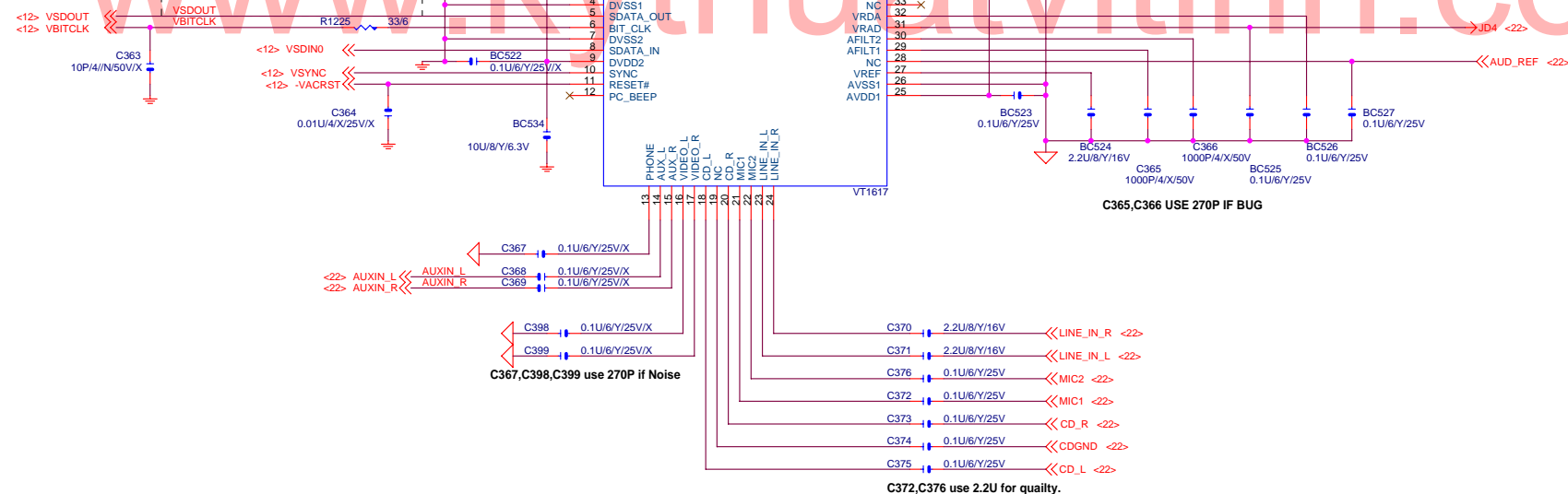


KBC/PS2



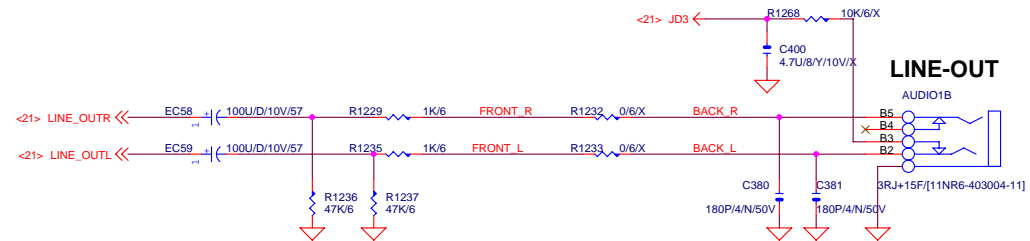
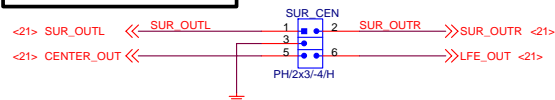


For VT1616/VT1617 SPDIFIN is not support
R1265 Default 4.7K.

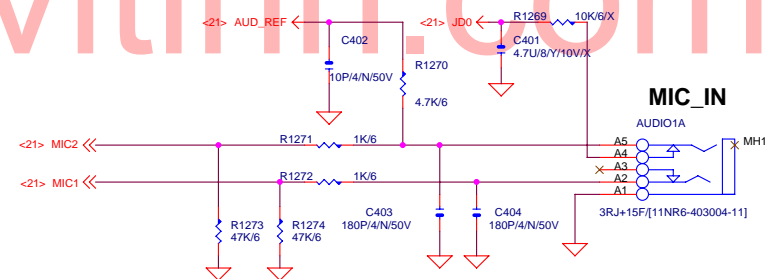
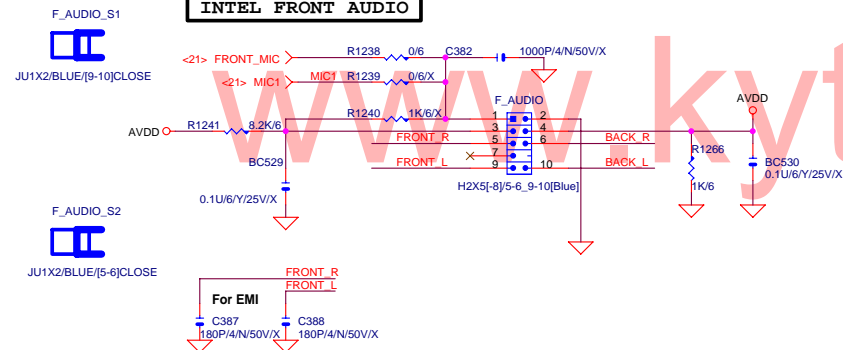


C372,C376 use 2.2U for quality.

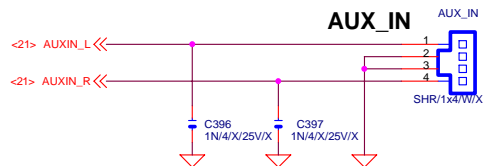
GBT 6 Chanel CONN



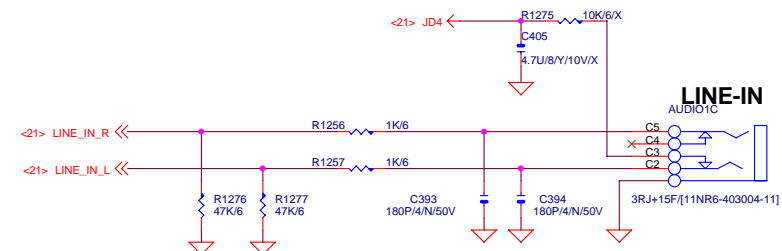
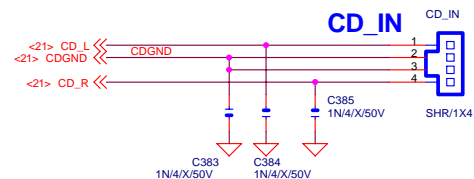
INTEL FRONT AUDIO



AUX_IN



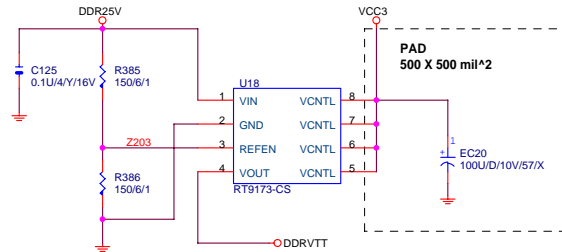
CD_IN



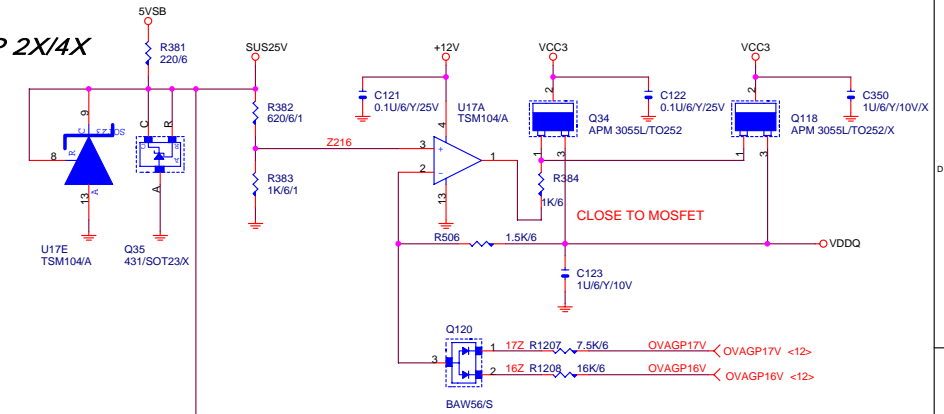
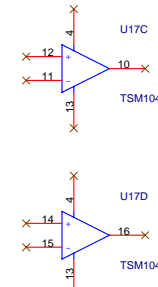
GIGABYTE

Title			AUDIO OUTPUT, GAME PORT
Size	Document Number	7VM400M-RZ	
Custom		Rev	1.0
Date:	星期二, 四月 27, 2004	Sheet	22 of 28

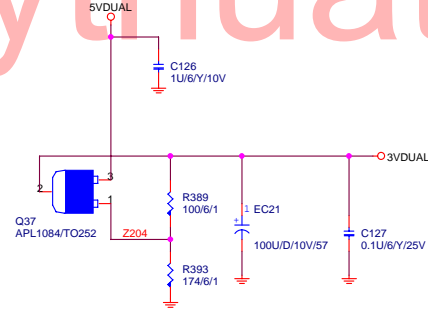
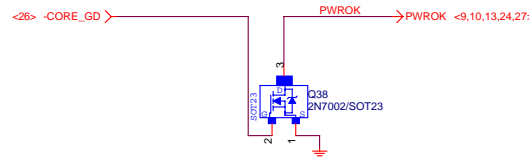
1.25V DDRVTT SWITCHING SOLUTION



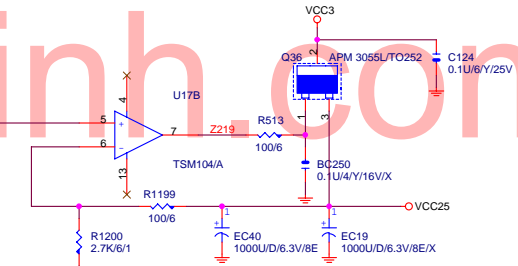
VDDQ 3.3V/1.5V FOR AGP 2X/4X



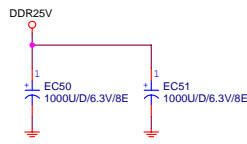
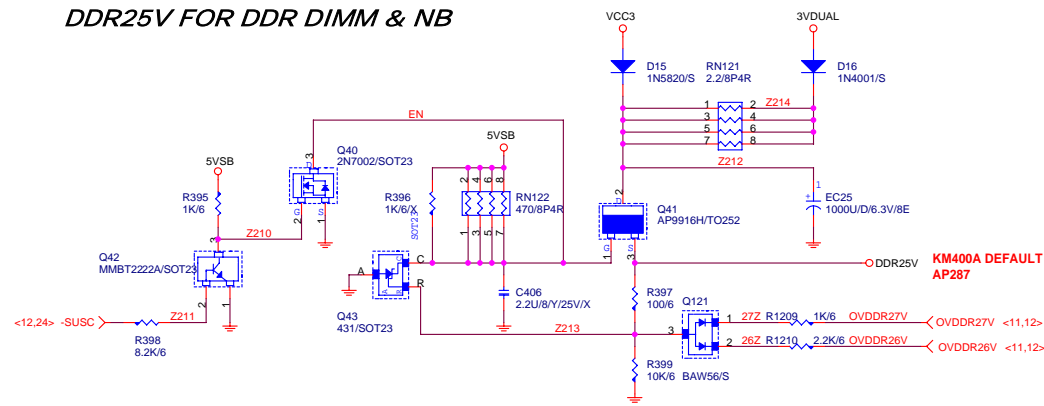
5VDUAL TRANS TO 3VDUAL(3.3V)



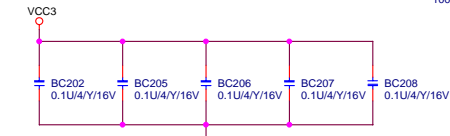
VCC25 FOR NB,SB,CK408,CKBF



DDR25V FOR DDR DIMM & NB



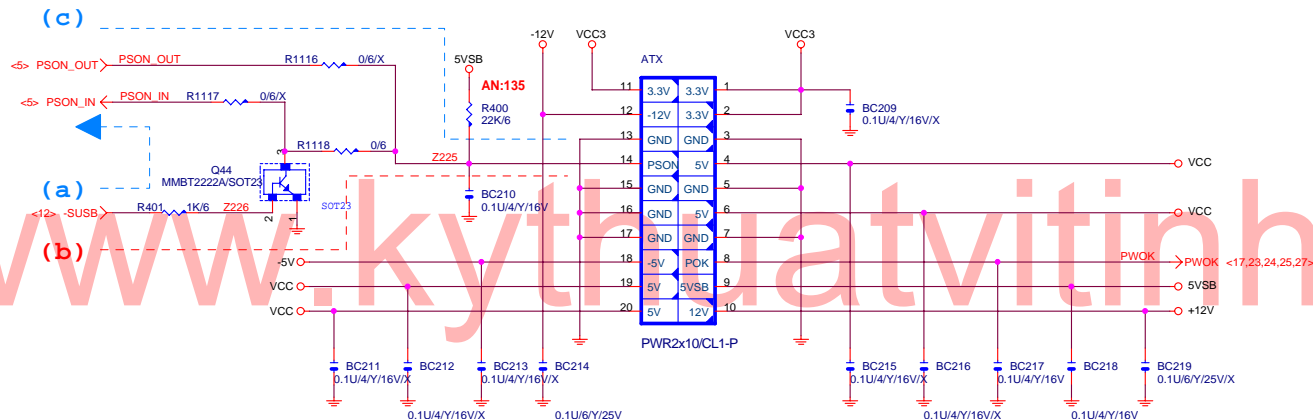
5VDUAL CIRCUIT



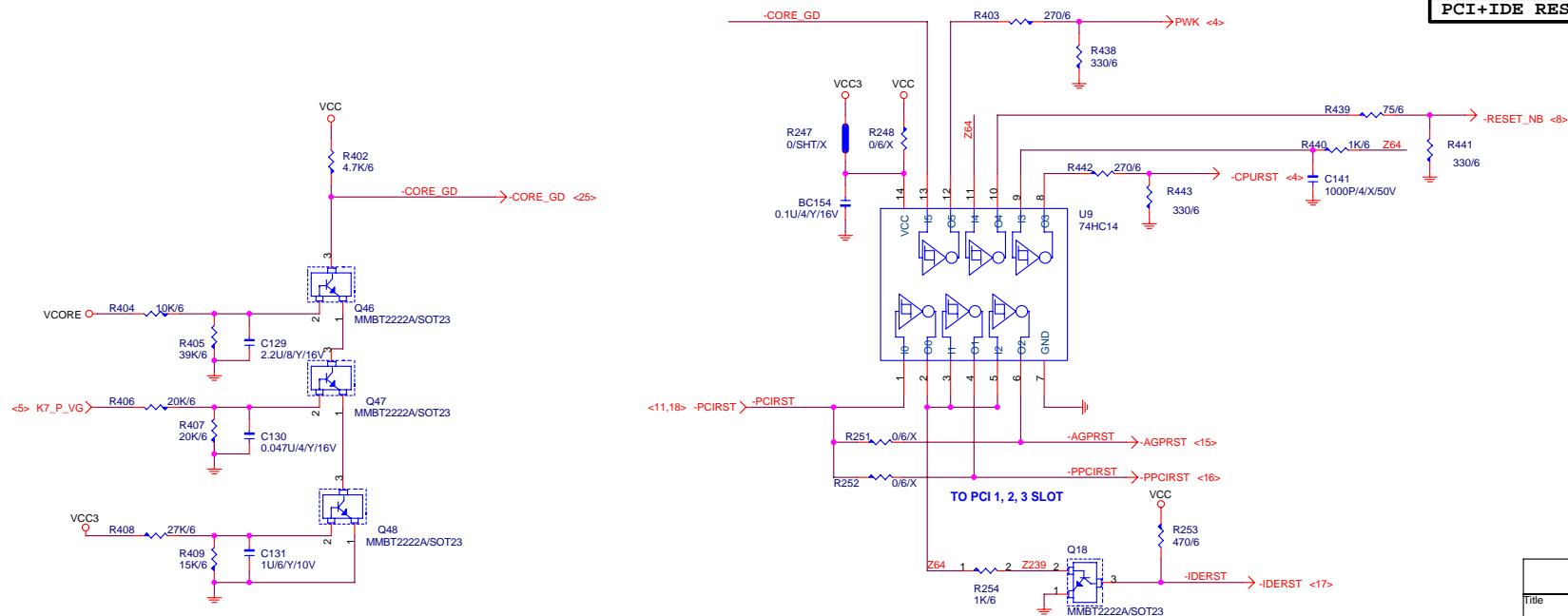
GIGABYTE			
Title	DDR POWER		
Size	Document Number	7VM400M-RZ	Rev 1.0
Date	星期二, 四月 27, 2004	Sheet 25	of 28

ATX CONN, DC POWER

ATX POWER CONNECTOR



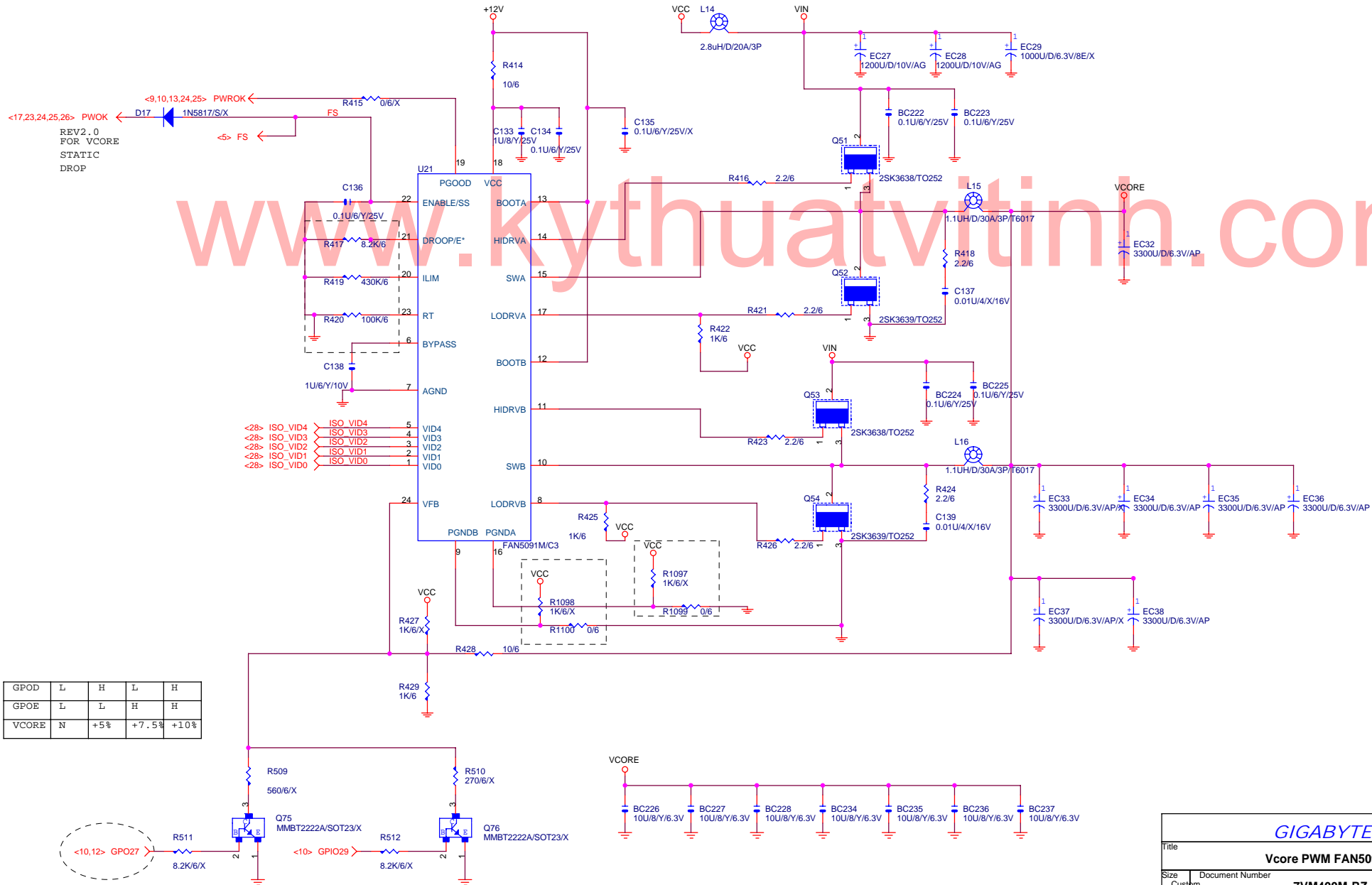
PCI+IDE RESET



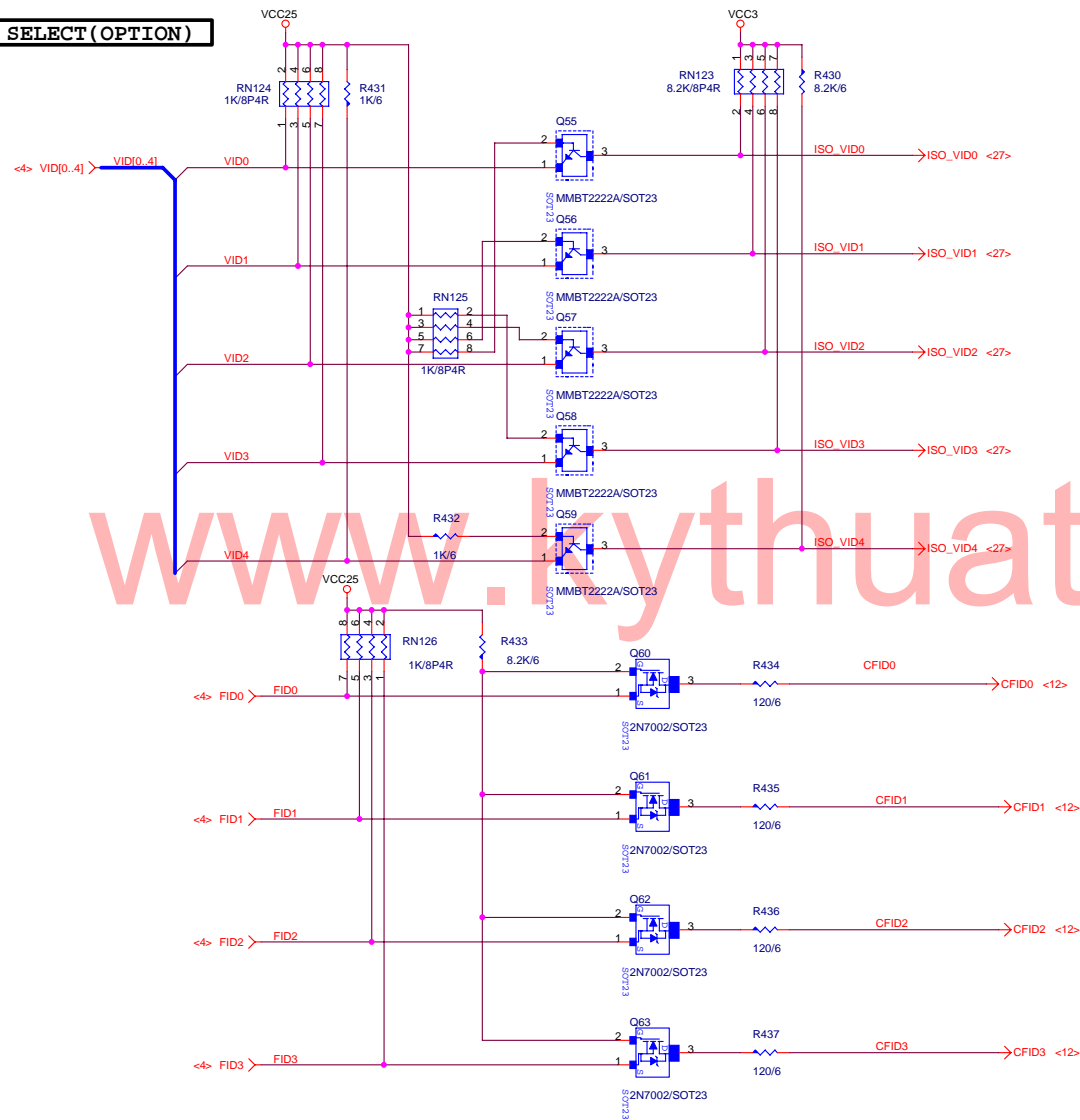
GIGABYTE

ATX, DC POWER

Size	Document Number	Rev
Custom	7VM400M-RZ	1.0
Date:	星期四, 四月 27, 2004	Sheet 26 of 28

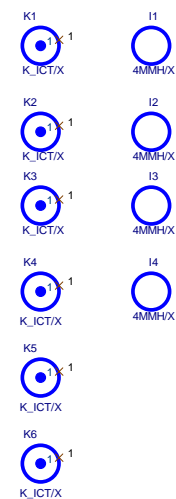
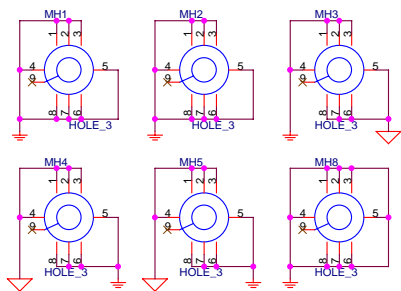


ID SELECT(OPTION)



VID[4..0]	VCC_CORE	VID[4..0]	VCC_CORE
00000	1.850	10000	1.450
00001	1.825	10001	1.425
00010	1.800	10010	1.400
00011	1.775	10011	1.375
00100	1.750	10100	1.350
00101	1.725	10101	1.325
00110	1.700	10110	1.300
00111	1.675	10111	1.275
01000	1.650	11000	1.250
01001	1.625	11001	1.225
01010	1.600	11010	1.200
01011	1.575	11011	1.175
01100	1.550	11100	1.150
01101	1.525	11101	1.125
01110	1.500	11110	1.100
01111	1.475	11111	

www.kythuavietinh.com



SW1 : Frequency Override.

O: ON X: OFF

RATIO	1	2	3	4	5
AUTO	X	X	X	X	O
5X	O	O	X	O	X
5.5X	X	O	X	O	X
6X	O	X	X	O	X
6.5X	X	X	X	O	X
7X	O	O	O	X	X
7.5X	X	O	O	X	X
8X	O	X	O	X	X
8.5X	X	X	O	X	X
9X	O	O	X	X	X
9.5X	X	O	X	X	X
10X	O	X	X	X	X
10.5X	X	X	X	X	X
11X	O	O	O	O	X
11.5X	X	O	O	O	X
12X	O	X	O	O	X
>=12.5X	X	X	O	O	X

GIGABYTE

VCORE VOLTAGE ADJUST			
Title	Document Number	Rev	1.0
Size	Custom	7VM400M-RZ	
Date:	星期二, 四月 27, 2004	Sheet	28 of 28